Remarks

Thorough examination by the Examiner is noted and appreciated. Applicants gratefully acknowledge indication of allowance of claims 13-19 and indication of allowable subject matter in claims 4, 5, 12, and 20. Claims 1-20 are pending in the Application. Claims 1-3 and 6-11 have been rejected.

The Specification has been amended to eliminate matter containing a typographical error.

The rejected claims have been amended to clarify Applicants invention and a new claim added to recite indicated allowable subject matter.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example, support for the amended claims is found in the Specification at paragraph 0017 and 0018:

Referring to Figure 1C, following the second polysilicon layer 18 deposition, the second polysilicon layer 18 is etched back in a dry etching process to a desired polysilicon layer thickness, for example having a thickness between about 1000 Angstroms and about 1500 Angstroms. Preferably a chemical dependent etching (CDE) process is used which includes a downstream etching process where the plasma is created upstream from the plasma wafer and transported down stream to contact the wafer where primarily chemically dependent etching takes place without plasma ion bombardment energies contributing to the etching process. The CDE process advantageously contributes to more uniform etching and **consequently a smoother polysilicon layer topography** without plasma etching damage such as micro-trenching of the polysilicon.

For example, it has been found that the deposition of a thicker than desired polysilicon second layer followed by an etchback process according to preferred embodiments results in a **lower profile angle of the polysilicon layer topography adjacent** the gate structure e.g., 12A and 12B at e.g., 20A, resulting in a less sharply cornered angle in a subsequently formed floating gate electrode area portion overlying the HTO layer 14C. **Such a relatively smoother polysilicon layer topography** formed by the etchback process **has been found** to be beneficial in both the electrical properties of read and write operations in a final floating gate structure, believed to be due to reducing a relatively higher electric field area (sharply cornered) in the floating gate structure. In addition, the **smoother polysilicon layer topography** reduces polysilicon etching residues in subsequent polysilicon dry etching operations, for example in defining the overlying polysilicon control gate, as well as avoiding residual etching deposition of the second interpoly layer on active areas as explained below."

Claim Rejections under 35 USC 112

The claims have been amended to overcome Examiners rejection.

Claim Rejections under 35 USC 102

1. Claims 1, 6, and 9-10 stand rejected under 35 USC 102(e) as being anticipated by Ding (USPUB 2004/0201059).

Ding discloses a nonvolatile memory device and method for forming the same.

In the method and device of Ding, Ding discloses where the floating gate is formed by depositing a polysilicon layer (first polysilicon layer) (item 160.1; paragraph 0067) **which is then planarized by CMP** to be co-planar with nitride overlying the select gate (paragraphs 0064, 0068; Figures 10-12). The first polysilicon layer is then etched without a mask to form a first portion of the floating gate (paragraph 0069). A second polysilicon layer (160.2) is then formed over the first polysilicon layer and etched to **form a second portion of the floating gate adjacent sidewall portions of the gate structure** (paragraphs 0071-0072).

In the method and device of Ding, the control gate is formed by depositing a third polysilicon layer (control gate polysilicon layer) (see e.g., item 170, Figures 18, 19, 20, 22A, paragraphs 0078 and 0079) over a dielectric layer (ONO) (item 164), the floating gate (items 160.1 and 160.2) and select gate (gate structure) (item 140). Ding teaches that the third polysilicon layer **is non planar and is formed with cavities** (item 170C, Figure 18, paragraph 0080) which are filled with silicon dioxide **and then planarized to form a planar layer of polysilicon** and silicon dioxide between protruding polysilicon portions (see Figure 19).

The control gate polysilicon layer is then etched without a mask selective to silicon dioxide to create second cavities (item 1810) (openings) in the polysilicon layer (see paragraph 0081; Figure 20). Ding teaches that the etch process can form cavities that extend through the ONO layer (as shown in Figure 20) or that the etch process can stop before or at the ONO layer (paragraph 0081). Ding also discloses (but does not show) that the top surface of the second polysilicon (control gate polysilicon) may be planar polysilicon (formed without the cavities) (paragraph 0082). Ding then teaches depositing a protective material **(hardmask material) (silicon nitride) over the polysilicon (into the cavities) and then planarizing the silicon nitride by CMP** to form a planar top surface of the silicon nitride (item 1910; Figure 21, paragraph 0083) leaving cavity portions in the silicon nitride (item 1810, Figure 21).

An ARC layer (item 2010; Figure 22A) is then deposited into the silicon nitride cavity portions (flowed on the surface and cured) to **form a planar top surface** (paragraph 0085). A lithographic patterning and etching process is then carried out to first etch through uncovered portions of the silicon nitride to form a silicon nitride etch mask (hard mask) (Figure 23; paragraph 0087). The oxide filling (item 1710) is then secondly etched away (paragraph 0088; Figure 24) followed by thirdly etching the second polysilicon layer **using the silicon nitride as an etch mask** to stop on the ONO (paragraph 0089; Figure 25) to form the control gate. A Fourth etch process is then carried out using the silicon nitride as an etch mask (hard mask)to etch through the ONO layer and the first polysilicon layer (item 160.1) to fully define the control gate and floating gate (paragraph 0090).

Thus, Ding does not disclose Applicants disclosed and claimed invention

Nowhere does Ding suggest, disclose, or teach:

"etching back the first polysilicon layer through a portion of the first polysilicon layer thickness according to a first dry etching process to partially smooth the first polysilicon layer topography;

or

"forming a second polysilicon layer over the second dielectric insulating layer; and,

then lithographically patterning and dry etching according to respective sequential dry etching processes **through a thickness portion of the respective second and first polysilicon layers** to respectively form third and second polysilicon gate electrodes.

Rather, the method of Ding teaches etching back the first polysilicon layer to form a first portion of the floating gate (below the first gate structure), forming a second polysilicon layer over the first floating gate portion; then etching the second polysilicon layer to form a second floating gate portion adjacent the sidewalls of the first gate structure; then forming a third polysilicon layer with a surface topography forming cavities, then filling the cavities with a hard mask material and then planarizing by CMP prior to etching a hard mask and **then** etching the control gate (third polysilicon layer) and floating gate (first polysilicon layer).

Thus Ding is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Further with respect to claim 10, nowhere does Ding disclose forming by his disclosed method the structure "wherein the third polysilicon gate electrode is formed comprising a first edge aligned with an underlying edge of the second polysilicon gate electrode **which is aligned over a portion of the first polysilicon gate electrode**".

Claim Rejections under 35 USC 103

2. Claims 3 and 7-8 stand rejected under 35 USC 103(a) as obvious over Ding, above.

Applicants reiterate the comments made above with respect to Ding.

As noted by Examiner, Ding does not disclose or suggest etching back the first polysilicon layer or that the first dielectric layer is silicon oxide. Applicants reject Examiners assertion of Official Notice that silicon dioxide may be used as the first dielectric layer where the prior art has not shown Applicants structure or method of forming the same. Rather Ding discloses etching the first polysilicon layer at or below a height of the gate structure and then forming a second polysilicon layer on the first polysilicon layer and then etching the second polysilicon layer to form sidewall portions along the gate structure.

Ding also discloses an entirely different solution to the problem of polysilicon surface topography. Ding discloses filling the cavities formed by the surface topography of the **control gate polysilicon layer** (third polysilicon layer) by depositing a hardmask material (silicon nitride) (and ARC material) within the cavities, which is then planarized by CMP prior to forming a hardmask and then etching the control gate polysilicon layer and the floating gate (first polysilicon layer portion) according to the hardmask.

Applicants have also pointed in the Specification at paragraph 0018 where the discovered advantages of the etchback process of the first polysilicon layer are outlined:

"For example, it has been found that the deposition of a thicker than desired polysilicon second layer followed by an etchback process according to preferred embodiments results in a lower profile angle of the polysilicon layer topography adjacent the gate structure e.g., 12A and 12B at e.g., 20A, resulting in a less sharply cornered angle in a subsequently formed floating gate electrode area portion overlying the HTO layer 14C. Such a relatively smoother polysilicon layer topography formed by the etchback process has been found to be beneficial in both the electrical properties of read and write operations in a final floating gate structure, believed to be due to reducing a relatively higher electric field area (sharply cornered) in the floating gate structure. In addition, the smoother polysilicon layer topography reduces polysilicon etching residues in subsequent polysilicon dry etching operations, for example in defining the overlying polysilicon control gate, as well as avoiding residual etching deposition of the second interpoly layer on active areas as explained below."

Thus, since Ding does not show Applicants process, but rather discloses a completely different process and method for forming the floating gate (third polysilicon gate electrode) and control gate (second polysilicon gate electrode) including a hardmask filling and a CMP planarization process, the teachings of Ding are insufficient to make out a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 2 and 11 stand rejected under 35 USC 103(a) as obvious over Ding, above, in view of Lam et al. (US 6,426,524).

Applicants reiterate the comments made above with respect to Ding.

The fact that Lam et al. discloses using a chemical downstream etching process in a process for forming an entirely different structure i.e., for forming square or vertical sidewall spacers (see Abstract; col 1, lines 9-54) does not further help Examiner in making out a *prima facie* case of obviousness.

Even assuming *arguendo* a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

Applicants gratefully acknowledge the allowance of claims 13-19 and have included new claim 21 including indicated allowable subject matter. Based on the foregoing, Applicants respectfully submit that the all of the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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